YIELD MAXIMIZATION IN THE MANUFACTURE OF INTEGRATED CIRCUITS

## Abstract of the Disclosure

A method and apparatus for improving the manufacturability of Integrated Circuits (ICs) formed on semiconductor dies is described. A plurality of different designs for some or all of the standard cells are made available to the circuit designer. Each different design may address a different problem associated with different manufacturing processes or a different design related yield limiter. Each of the design variants is characterized indicating its relative ease of manufacture, or it's yield sensitivity to certain IC design factors. The designer, typically with assistance from computer aided tools, can then select the standard cell variant for each of the cell used in the IC design that best addresses his or her design constraints. In other embodiments, variant versions of I/O cells and memory cells could also be created and made available to the designer in a similar fashion.